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FOR

METHOD AND APPARATUS FOR AUTOMATIC FAST LOCKING POWER CONSERVING SYNTHESIZER

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METHOD AND APPARATUS FOR AUTOMATIC FAST LOCKING POWER
CONSERVING SYNTHESIZER

Field

The invention pertains to a frequency synthesizer device and in particular to a frequency synthesizer device with a fast off-to-lock time to enable cycled or intermittent operation and achieve power savings.

Background

Power consumption is an important factor in the design of many electronic devices. Often, these devices must operate on a limited power supply. For example, devices such as mobile and wireless phones, mobile computers, and other devices are generally battery operated. To maximize the operating time in between changing or recharging batteries, mobile devices are often designed with low power consumption components and power saving features. In other applications, it is desirable to minimize the power consumption of devices, mobile and non-mobile, to reduce operating costs and/or extend the life of the devices and/or their components.

Many mobile devices include wireless communication devices and interfaces to send and receive data. These wireless communication devices and interfaces are often a significant source of power consumption. Various forms of wireless or over-the-air communication systems, including radio transmissions, have been employed.

Some of these mobile device have more than one mode of operation, including modes specifically designed to conserve power. Power saving modes vary in the extent that a device's components are cycled or powered off. These power saving modes are typically referred to by various names including standby mode, sleep mode, and idle mode. For purposes of this application, these terms may be used interchangeably to refer to a power savings mode where one or more components of the

device are reconfigured to consume less power than during normal operation or no power at all.

Generally, radio communication systems include a radio (modem) device to transmit and receive signals, and a control unit to control the operation of the radio device.

Synthesizers are commonly employed within radio devices to lock on an operating, carrier, or transmission frequency. The terms operating frequency, carrier frequency, or transmission frequency are herein used interchangeably to mean the frequency or channel on which communications are received or transmitted.

Conventional synthesizers typically have relatively long tuning times when powered On. The synthesizer tuning time includes the time it takes the synthesizer to reach stable operation at a particular frequency. Some conventional synthesizers are implemented using a phase-lock-loop (PLL) design. One tuning delay, known as the channel-to-channel lock time, for a PLL-based synthesizer includes the time it takes to lock onto a desired frequency and phase. If a synthesizer is not able to power On and lock onto the desired operating frequency within a maximum time period, then a device may miss receiving or transmitting data.

One cause of tuning delays when a conventional PLL-based synthesizer is first powered On or changes operating frequencies is that the tuning time is not determinable or predictable because the initial phase is unknown and/or random. That is, the synthesizer may take a relatively short time, or a relatively long time beyond a maximum channel-to-channel time, to lock onto the desired frequency and phase.

One way to avoid missed transmissions is to keep the synthesizer powered On at all times, thereby avoiding power On delays. However, this is contrary to power efficiency since the synthesizer would drain needed power even when no transmissions are expected. Another scheme to avoid missed transmissions is to power On the synthesizer early enough to

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permit it to be operational by the time a transmission is expected. This typically requires that an external system, such as a control unit, manage and monitor the operation of the synthesizer. This adds complexity to the design of a
5 communication system.

Therefore, there is a need for a synthesizer system with relatively short and predictable tuning times to achieve savings in average power consumption and that is simple to integrate into existing control units.

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BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a communication device utilizing the automatic fast locking power conserving synthesizer illustrating one embodiment of the invention.

Figure 2A is a block diagram of a master and slave communication scheme utilizing the automatic fast locking power conserving synthesizer illustrating one embodiment of the invention.

Figure 2B is a waveform diagram of transmit and receive time slots for the master and slave communication scheme illustrated in Figure 2A.

Figure 3 is a block diagram of a radio device utilizing the automatic fast locking power conserving synthesizer illustrating another embodiment of the invention.

Figure 4 is a block diagram of one embodiment of the automatic fast locking power conserving synthesizer.

Figure 5 is a waveform diagram illustrating the operating sequence of control signals of one embodiment of the automatic fast locking power conserving synthesizer.

Figure 6 is a waveform diagram illustrating the off-to-lock sequence for one embodiment of the automatic fast locking power conserving synthesizer.

Figure 7 is a flowchart of steps in a control sequence for one method of one embodiment of the automatic fast locking power conserving synthesizer.

Figure 8 is a flowchart of steps in a control sequence for another method of one embodiment of the automatic fast locking power conserving synthesizer.

Figure 9 is a block diagram of one embodiment of a main frequency divider as may be employed in one embodiment of the automatic fast locking power conserving synthesizer.

DETAILED DESCRIPTION

In the following detailed description of the invention, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, one skilled in the art would recognize that the invention may be practiced without these specific details. In other instances well known methods, procedures, components, and circuits have not been described in detail so as not to unnecessarily obscure aspects of the invention.

One aspect of the invention provides a frequency synthesizer that achieves a relatively fast off-to-lock time by controlling the sequence of how various components of the synthesizer are reactivated. The off-to-lock time is defined as the time it takes a synthesizer to become operational and lock to a channel, carrier, or operating frequency once it is activated, reactivated, or powered On, and may include settling time and/or tuning time. The relatively fast off-to-lock time permits the synthesizer to conserve power by internally cycling power to one or more of its components. The frequency synthesizer is capable of automatically controlling its internal power cycling by triggering from an externally generated signal to activate or deactivate one or more components of the synthesizer device. As used herein, the terms deactivate, power Off, and disable may be used interchangeably unless otherwise specified or understood by context; the terms activate, reactivate, power On, enable, and re-enable may also be used interchangeably unless otherwise specified or understood by context.

Figure 1 is a block diagram of a communication device utilizing the automatic fast locking power conserving synthesizer illustrating one embodiment of the invention. The communication device 102 may be either a master or slave device to transmit and/or receive data over one or more

channels. The communication device 102 may be employed as part of various electronic devices including mobile computers, wireless phones, wireless headsets, hand held electronic devices, and other devices that are part of a communication system.

5 system.

In one embodiment, the communication device 102 includes a control unit 104 and a radio (modem) device 106. The control unit 104 may include a baseband controller to manage the operation of the radio (modem) device 106. The radio (modem) device 106 generally performs as a transceiver, or a transmitter and/or receiver, to transmit and receive communications.

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As illustrated in Figure 2A, a wireless communication scheme may include a master device 202 and a slave device 204. Both the master device 202 and the slave device 204 include a communication device 102 which includes a radio device 106 to receive and transmit. The master device 202 initiates transmissions and controls when and/or if a slave device 204 may transmit. A slave device 204 typically awaits for transmissions from the master device 202.

In some wireless communication systems, communication devices, master or slave devices, may not transmit and receive simultaneously. Ordinarily, the master device 202 establishes time slots, illustrated in Figure 2B, in which it may transmit (TXm) and other time slots in which it receives (RXm) communications. Similarly, based on the time slots established by the master device 202, the slave device 204 may transmit (TXs) when the master device 202 is receiving (RXm) and receive (RXs) when the master device 202 is transmitting (TXm). Usually, a slave device 204 may not initiate transmissions unless enabled by the master device 202. There may be idle time in between time slots where no transmissions take place.

35 Typically, slave devices 204 keep their receivers powered
On to detect and receive transmissions from a master device

202. Keeping a slave device's receiver powered On wastes precious power if the master device 202 only transmit during known periodic time slots as illustrated in Figure 2B.

One power saving scheme relies on a duty cycle, turning Off a device's receiver during those time slots when transmissions are not expected. Typically, cycling a radio device to conserve power includes turning the radio device's synthesizer Off and On intermittently, thereby reducing the average power consumption of the synthesizer. However, in order to receive and/or transmit communications, a receiver or transmitter that has been powered Off needs to power On and lock to a carrier frequency.

Many communication standards specify the maximum duration of a time slot for master 202 and/or slave devices 204. This limits a device synthesizer's off-to-lock time, the amount of time that a powered Off radio device 106 and/or synthesizer has to power On and lock onto a transmission, carrier, or operating frequency. However, conventional synthesizers typically have relatively long off-to-lock times compared with their channel-to-channel lock times. Thus, it may not be possible to cycle a conventional synthesizer, power it Off then power it On and lock it to a carrier frequency, within a maximum defined time period in a predictable and deterministic manner.

Some communication standards or systems, including General Packet Rate System (GPRS) and Bluetooth Specification v.1.1, implement a channel hopping scheme where transmission frequencies change every time slot sequence. Typically, a Channel Jump signal is generated and a new transmission frequency is indicated to the radio device 106. Thus, a communication device 102 that turns its radio receiver Off intermittently or cycles to conserve power must be able to reactivate its receiver, turning it back On and locking to a new carrier frequency, quickly enough to receive transmissions. This is difficult to do with a maximum off-to-

lock time of as short as two hundred micro-seconds (200 μ sec.).

Figure 3 illustrates one embodiment of the radio (modem) device 106. Typically, the radio device 106 receives and transmits data wirelessly over a radio interface (Radio I/O). The radio device 106 includes an automatic fast locking power conserving synthesizer 302 to tune to an operating or carrier frequency or channel for transmitting and/or receiving communications. The radio device 106 may also receive one or more control signals to configure the radio device 106. The embodiment of the radio device 106 illustrated in Figure 3, may receive a Channel Jump signal which indicates a hop or change in the carrier frequency or channel, and a New Transmission Channel signal which indicates the operating or carrier frequency. The synthesizer 302 is capable of changing carrier frequencies, or frequency hop, during operation.

Figure 4 is a block diagram of a radio device utilizing the automatic fast locking power conserving synthesizer 302 illustrating another embodiment of the invention. The synthesizer 302 is configured as a phase locked loop (PLL) and includes a phase frequency detector 402, a charge pump 404, a loop filter 406, a voltage controlled oscillator (VCO) 408, a main frequency divider (M) 410, and a reference frequency divider (R) 412. The main frequency divider 410 and reference frequency divider 412 may be implemented as counters and/or modulus scalers, to scale an input frequency by a chosen value, and may be digitally configured.

Ordinarily, a reference frequency (fRef) is provided to the synthesizer 302 to lock on a desired carrier frequency. The output frequency of the synthesizer 302 is taken as the output frequency of the voltage controlled oscillator (fVCO) 408 and is given as $f_{VCO} = (M/R) \times f_{Ref}$, where M is the dividing value of the main frequency divider 410 and R is the dividing value of the reference frequency divider 412. In one embodiment of the synthesizer, the voltage controlled

oscillator output frequency f_{VCO} may be approximately 2.5 GHz. In various implementations, the main frequency divider M 410 and/or reference frequency divider R 412 may be programmable or configurable to a desired dividing value.

5 The phase frequency detector 402 compares two input signal frequencies and generates an output signal that is a measure of their phase difference. Generally, if the phase of a reference frequency (f_{Ref}) does not equal the phase of the output frequency from the voltage controlled oscillator 408 (f_{VCO}) the phase frequency detector 402 together with the charge pump 404 and loop filter 406 generate a direct-current (DC) or low-frequency phase-error signal that causes the VCO output frequency (f_{VCO}) to deviate in the direction of f_{Ref}.

10 The voltage controlled oscillator (VCO) 408 is an oscillator whose frequency is proportional to an applied input voltage representing the phase-error signal. Thus, the voltage controlled oscillator 408 reacts to the phase-error signal and causes the phase of its output frequency f_{VCO} to move towards the phase of the reference frequency f_{Ref}. In this manner, the voltage controlled oscillator 408 eventually locks onto f_{Ref}, thereby maintaining a fixed phase relationship between f_{VCO} and the reference frequency f_{Ref}.
15 In one implementation, once the voltage controlled oscillator 408 locks onto f_{Ref}, the error-signal from the phase frequency detector 402, charge pump 404, and loop filter 406 to the voltage controlled oscillator 408 is a relatively constant DC signal.

20 The source of the reference frequency f_{Ref} may be any device capable of generating a reference signal of desired frequency characteristics. In one embodiment, the reference frequency source may be a crystal oscillator. According to one embodiment, the reference frequency source may stay powered even when the radio device 106 and/or synthesizer 302 are powered off or placed in standby mode.

The charge pump 404, a phase-to-charge converter, acts like a level-shifter or amplifier serving to boost the signal from the phase frequency detector 402. Typically, the loop filter 406 may be a low-pass filter to remove high frequency components in the phase-error signal. In one implementation, the loop filter 406 may be designed as a third order type II PLL. According to one embodiment, the loop filter 406 may include sufficient capacitance to hold a voltage charge for at least several hundred micro-seconds even if the synthesizer 302 is powered Off. This capacitance may retain the voltage charge corresponding to the last operating frequency of the synthesizer 302.

The synthesizer 302 may also include logic devices to turn On and Off, or activate and deactivate, various components of the synthesizer 302.

Generally, upon powering On or restarting the synthesizer 302 it operates in open loop with the phase frequency detector 402 and main frequency divider 410 disabled. The voltage controlled oscillator 408 is enabled and operates at the frequency at which it operated before the synthesizer 302 was powered Off or disabled. The voltage controlled oscillator 408 may generate its previous operating frequency by using the retained voltage charge in the loop filter 406 capacitance. The main frequency divider 410 is then enabled such that its phase initially lags the phase of the reference frequency divider 412. In one implementation, the signal phase of the main frequency divider 410 initially lags the signal phase of the reference frequency divider 412 by a known phase difference. Thus, by controlling the reference frequency divider 412 and main frequency divider 410 relative to each other the phase frequency detector 402 can be reset and enabled (closed-loop operation) into a known state such that the synthesizer 312 can lock onto a phase and frequency in a predictable deterministic way.

According to one implementation, the initial phase lag of the signal from the main frequency divider 410 is a delay of the sum of a) logic gate delay(s) and b) a maximum number of cycles of the input signal, i.e. fVCO, to the main frequency divider 410. The delay caused by the logic gate(s) and maximum number of input signal cycles may vary according the various implementations of the main frequency divider 410. In one implementation, the delay caused by the logic gates (i.e. within the main frequency divider 410) may be changed by the choice, number, and configuration of logic gate(s) employed. In another embodiment, the delay or phase lag may be fine tuned by delaying a maximum number of input frequency cycles (i.e. fVCO) before outputting a signal from the main frequency divider 410.

Figure 9 illustrates one embodiment of a main frequency divider 410' including a multi-modulus prescaler frequency divider 422, which may be a dual modulus divider, coupled in series with a fully programmable frequency divider 424 which can be programmed to produce an output signal of desired frequency (i.e. fVCO/M). In one embodiment, the modulus (divisor value) for the prescaler frequency divider 422 may be between 16 and 128. According to one implementation, the prescaler frequency divider 422 has dual modulus 32 and 33.

The maximum number of input frequency cycles delayed by the main frequency divider 410' is determined by the modulus value of the prescaler frequency divider 422. Where the modulus value (divisor value) is 32, for example, the prescaler divider 422 causes a delay of 32 input cycles (input signal fVCO) before a first output cycle (output signal fVCO/M) is generated. Thus, upon enabling the main frequency divider 410' the initial phase lag is a known amount, including logic delays and the prescaler frequency divider delay. As illustrated in Figure 4, the voltage controlled oscillator 408 may receive an Enable Synthesizer signal to turn On and/or Off the voltage controlled oscillator 408. A

first D flip flop 414 serves to reset the main frequency divider 410 based on a Reset Synthesizer signal which is clocked by an output signal fRef/R from the output of the reference frequency divider 412. In one embodiment, the output signal fRef/R from the reference frequency divider 412 clocks the Reset Synthesizer signal to the main frequency divider 410 on a rising edge. A second D flip flop 416 serves to reset the phase frequency detector 402 based on a Reset Synthesizer signal when clocked by the output signal fVCO/M from the main frequency divider 410 thereby enabling the operation of the phase frequency detector 402. In one embodiment, the fVCO/M output signal from the main frequency divider 410 clocks the Reset Synthesizer signal to the phase frequency detector 402 on a rising edge.

The synthesizer 302 may be set to power savings mode, or standby, by turning the power Off to one or more of its components. The synthesizer 302 may be cycled, or powered Off and On intermittently, while the radio device 106 is not in use to conserve power. In Figure 3 for instance, the voltage controlled oscillator 408 may be powered Off and On via an Enable Synthesizer signal. Generally, the synthesizer 302 remains powered On while it transmits and receives transmissions. The synthesizer 302 is powered Off in between transmit and receive time slots, during those receive time slots when no transmissions from another device are expected, when it is done receiving, during those transmit time slots when it has nothing to transmit, and when it is done transmitting. For example, in one embodiment, the synthesizer 302 is powered Off after a listening period before the end of a receive time slot when it is determined that no transmissions are likely to occur.

The synthesizer 302 is incorporated into the radio device 106 and may be configured to conserve power. Prior to receiving or transmitting, the radio device 106 is activated or powered On. It may be activated as a result of an external

signal such as the Channel Jump signal. The Channel Jump signal may be used in a channel hopping communication system to indicate that the radio device 106 should change to a new frequency or channel.

5 While one embodiment of the invention is shown in Figure 4, it must be understood that the invention may be practiced in other embodiments without deviating from the invention. For example, the synthesizer 302 may be implemented as an integer-N synthesizer.

10 Figure 5 illustrates waveform diagrams showing the operation and timing sequence of control signals of one embodiment of the synthesizer 302. While Figure 5 provides a general description of the operation of the control signals, a more detailed view of the timing sequence of one embodiment of the synthesizer 302 is given in Figure 6.

15 The Channel Jump signal, or any other chosen external signal, may trigger radio device 106 to generate one or more internal signals to restart or reactivate the synthesizer 302. Thus, the radio device 106 and/or the synthesizer 302 may automatically cycle its power. Since the radio device 106 internally controls when and how the synthesizer 302 and/or its components are cycled, the control unit 104 which controls the radio device 106 need not be aware of the power cycling of the synthesizer 302.

20 The radio device 106 internally generates an Enable Synthesizer signal at time t_1 , after the Channel Jump signal has been detected, to activate or power On one or more of its components such as the voltage controlled oscillator 408. The voltage controlled oscillator 408 operates in open loop since at time t_1 the outputs of the phase frequency detector 402 and main frequency divider 410 are disabled. In open loop, the operating frequency of the voltage controlled oscillator 408 may be its previous operating frequency before being deactivated or powered Off and may be generated by using the retained voltage charge in the loop filter 406 capacitance.

Once the voltage controlled oscillator 408 has settled or stabilized, a Reset Synthesizer signal is generated by the radio device 106 at time t2 to reset one or more components of the radio device such as the phase frequency detector 402 and main frequency divider 410.

Once the radio device 106 has been properly activated it may receive and/or transmit between time t3 and time t4.

When the communication time slot ends at time t4, the radio device 106 may again change to standby mode. To change to standby mode, the Reset Synthesizer signal may be used to deactivate or disable synthesizer components such as the main frequency divider 410 and phase frequency detector 402 at time t5. The Enable Synthesizer signal at time t6 may then disable or power Off the voltage controlled oscillator 408 and/or other components of the radio device 106. Note that by shutting Off the synthesizer components in this order the voltage charge corresponding to the last operating frequency may be retained or stored in the capacitance of the loop filter 406.

This cycle may be repeated again after a standby period from time t6 to time t7. During this standby period, one or more synthesizer components may be powered Off or disabled to conserve power. Time t7 corresponds to the beginning of a new cycle similar to the cycle beginning at time t1.

As noted above, it is particularly important that once the synthesizer 302 is restarted it is able to lock onto the operating or carrier frequency in a relatively short period of time.

The invention permits a synthesizer 302 to restart operations in a relatively short off-to-lock time. By restarting the different components of the synthesizer 302 in a certain sequence, the invention permits the synthesizer 302 to be cycled intermittently between On and Off and still transmit and receive transmissions.

Figure 6 is a waveform diagram illustrating the off-to-lock sequence for one embodiment of the automatic fast locking power conserving synthesizer 302. This diagram represents a more detailed view of the synthesizer operation during time t_1 to time t_3 illustrated in Figure 5. The timing sequences also correspond to the embodiment of the synthesizer 302 illustrated in Figure 3 and generally described above.

Generally, the synthesizer restart or power On process illustrated in Figure 6 first starts the synthesizer 302 at the frequency at which it operated prior to being powered Off, and then changes to a new operating frequency. By starting the synthesizer 302 at the previous operating frequency, the delays associated with locking onto a frequency and phase after restarting a synthesizer are substantially reduced.

Referring to Figure 6, at some time prior to time t_0 , the Transmission Channel signal indicates, directly or indirectly, the transition 602 from a first carrier frequency Channel A to a second carrier frequency Channel B. The Transmission Channel signal may be used to change the value and/or configuration of one or more components of the synthesizer such as the phase frequency detector 402, Reference Frequency Divider 412 and/or the Main Frequency Divider 410. According to one embodiment, the Transmission Channel signal serves to configure the phase frequency detector 402 and Main Frequency Divider 410. In one implementation, the Transmission Channel signal may provide a new reference frequency f_{Ref} for the synthesizer 302.

Prior to time t_0 , certain synthesizer components are disabled or powered Off. For instance, at time t_0 the phase frequency detector 402, main frequency divider 410, and voltage controlled oscillator 408 are disabled and not providing an output signal.

At time t_0 , a Channel Jump signal 606, or its equivalent, is sent to the radio device 106. As noted above, the radio device 106 may use the Channel Jump signal to generate one or

more internal signals to the synthesizer 302. Upon the occurrence of a Channel Jump signal 606, the radio device 106 generates an Enable Synthesizer signal 608 to enable or power On components of the synthesizer 302 that may have been 5 powered Off. For instance, at time t_1 the voltage controlled oscillator 408 is restarted by the Enable Synthesizer signal 608. A time period between time t_1 and time t_2 may serve to allow the voltage controlled oscillator 408 to reach stable oscillation.

10 After stable oscillation has been reached but before the loop is closed at time t_2'' , the voltage controlled oscillator 402 sets its initial operating frequency from the retained voltage charge in the loop filter capacitance. The loop filter 406 may have sufficient capacitance to maintain a voltage charge for at least the time interval during which the synthesizer 302 is powered Off in between time slots; time t_4 to time t_8 in Figure 5 for instance. Thus, the loop filter 406 may serve as a memory to store the DC voltage corresponding to the last operating frequency prior to 15 powering Off the synthesizer 302.

20 At time t_2 , after the voltage controlled oscillator 408 is powered On and allowed to stabilize its oscillation, a Reset Synthesizer signal 610 is generated by the radio device 106. The Reset Synthesizer signal 610 serves to initialize 25 and start the main frequency divider 410 and phase frequency detector 402. However, the start of these components 410 and 402 is delayed and synchronized by logic devices 414 and 416. Meanwhile, the outputs of the phase frequency detector 402 and main frequency divider 410 remain disabled with the 30 synthesizer 302 operating in open loop.

35 Just after time t_2 , a Channel Select signal is generated by the radio device 106. This signal serves to initialize the phase frequency detector 402 and main frequency divider 410 to their previous operating values or settings before the synthesizer was powered Off or disabled. While the phase

frequency detector 402 and main frequency divider 410 are initialized, their output remains disabled.

At time t_2' , the first D flip flop 414 clocks in the Reset Synthesizer signal 610 upon the first rising edge of the output signal 614 from the reference frequency divider 412 thereby resetting Reset M 624 and enabling the operation and output of the main frequency divider 410. A short time later, the second D flip flop 416 clocks-in the Reset Synthesizer signal 610 to Reset PFD 626 and enable the operation and output of the phase frequency detector 402. After enabling the phase frequency detector 402, the synthesizer 302 operates in closed loop although no Phase-Error signal is generated until the phase frequency detector 402 receives signals from the reference frequency divider 412 and the main frequency divider 410.

By disabling the phase frequency detector 402 while its input signals are setup, this reduces the amount of time it would take to lock onto the phase of the carrier or operating frequency. That is, the sequence in which the input signals fRef/R and fVCO/M arrive to the phase frequency detector 402 is controlled to provide predictable performance upon starting the phase frequency detector 402.

Starting at time t_2'' , the phase frequency detector 402 detects the signal from the reference frequency divider 618; then a short time later 620 the phase frequency detector 402 detects the signal from the main frequency divider 410. The phase frequency detector 402 may then compare the phase difference/error between the reference frequency divider signal and the main frequency divider signal and generate a phase-error signal to the voltage controlled oscillator 408 calculated to lock its two inputs into phase. Because the reference frequency signal fRef/R reaches the phase frequency detector first 618, followed by the feedback signal fVCO/M 620, the phase frequency detector 402 is able to take the shortest route to bringing the signals into phase. This known

systematic initial phase error 632, from times 618 to 620, allows the synthesizer 302 to phase lock in a predictable fashion.

By coarsely locking onto the previous operating frequency, the synthesizer 302 is able to bring its two input signals into phase much quicker than it otherwise would. This reduces the time it takes to change and lock onto a new frequency.

The synthesizer 302 may then generate a second Channel Select signal 522 at time t_3' to change from the previous operating frequency to a new operating frequency. This second Channel Select signal 622 may occur after the reference frequency divider 412 signal and the main frequency divider 410 signal are coarsely or substantially, but not necessarily completely, locked in phase. This reduces the time it takes to jump to the next channel.

Changing to the next transmission channel at time t_3' may be accomplished by reconfiguring one or more components such as the phase frequency detector 402 and/or the main frequency divider 410.

According to one embodiment, the reference frequency f_{Ref} is generated by a source which is continually powered On even when the radio device 106 is disabled or turned Off. By keeping the reference frequency source powered On, this reduces the restart time of the synthesizer 302 since it avoids the settling time delays of the reference frequency source.

Generally, this start sequence takes less time than it would otherwise take to start the synthesizer 302 without controlling the order in which the synthesizer components are restarted. In one implementation, the time it takes to start the synthesizer 302 and lock into the new channel or carrier frequency is less than or equal to two hundred micro-seconds (200 μ sec.). In the embodiment illustrated in Figure 6, this may be the time period between time t_1 when the Channel Jump

signal is received and time t_3 when the synthesizer 302 is ready to transmit or receive.

Figure 7 is a flowchart of a control sequence for the steps of one method of one embodiment of the automatic fast locking power conserving synthesizer 302. Once the synthesizer 302 is disabled, in standby mode, or in power saving mode, the restart process may be triggered by a jump channel request at step 702 by an external device, such as a baseband controller. This enables one or more components of the synthesizer 302 to jump to the operating frequency of the synthesizer 302 before it was turned off or placed in standby or sleep mode at step 704. Then at step 706, the synthesizer 302 is allowed to coarsely lock the phase of its output to a reference signal. Once a coarse lock has been achieved, a jump to the desired operating frequency occurs at step 708. After a settling time, the synthesizer 302 locks to a desired operating frequency at step 710. Then the synthesizer 302 is ready to receive or transmit on the new operating frequency at step 712.

According to one implementation of this invention, the synthesizer method and/or apparatus need not first coarsely lock to the previous operating frequency. Rather, the invention may be practiced by starting the synthesizer at a desired operating frequency. Such would be the case when the synthesizer is first powered on after a long time for instance.

Figure 8 illustrates a method of how the invention may be practiced without first locking to the previous operating frequency. Note that this method applies equally to an apparatus such as that shown in Figure 4. A jump request is interpreted as a command for the synthesizer to wakeup 802. As before, the voltage controlled oscillator is enabled for operation 804. Since the main frequency divider 410 and phase frequency detector 402 remain disabled, the synthesizer 302 operates in open loop. The main frequency divider 410 and

phase frequency detector 402 are initialized to operate at the desired frequency 806. However, they remain disabled and not providing an output signal. As before, the main frequency divider 410 is enabled so that the phase of its output signal lags the phase of the reference frequency divider 412 signal 808. According to one implementation, the main frequency divider 410 output signal lags initially the reference frequency divider 412 output signal by a known amount, i.e. 632 in Fig. 6. The phase frequency detector is then enabled 10 810 so that the synthesizer operates in closed loop. The synthesizer is then ready to transmit or receive at the desired operating frequency.

This starting sequence generally allows the synthesizer to lock onto a phase quicker than it otherwise would. For example, if the phase frequency detector 402 had been started with the phase of the signal from the main frequency divider 410 leading the phase of the signal from the reference frequency divider 412 by one degree, it would have taken three hundred and fifty-nine degrees to phase lock. By guaranteeing that the phase from the main frequency divider 410 initially slightly lags the phase of signal from the reference frequency divider 412, the time to phase lock can be substantially reduced. In various embodiments, the initial phase difference between the signals from the main frequency divider 410 and reference frequency divider 412 may be an unknown amount, an unknown amount within a range, or a known amount.

The synthesizer 302 may be embodied in one or more integrated circuit devices. Parts of the synthesizer restarting scheme describe above may be implemented by 30 software. This process and apparatus may also serve as a means to conserve power.

While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not 35 restrictive on the broad invention, and that this invention

not be limited to the specific constructions and arrangements shown and described, since various other modifications may occur to those ordinarily skilled in the art. For example, the invention has been described herein with reference to a channel hopping communication system. Other kinds of communication systems may be used. Additionally, the invention has been described for restarting the synthesizer on a channel jump signal but it is equally applicable to restarting the synthesizer on many other signals.

Additionally, it is possible to implement the invention or some of its features in hardware, firmware, software or a combination thereof where the software is provided in a processor readable storage medium such as a magnetic, optical, or semiconductor storage medium.